MULTIMEDIA **UNIVERSITY**

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FINAL EXAMINATION

TRIMESTER 2, 2017/2018

DMT5018 – MICROCONTROLLER TECHNOLOGY
(Diploma in Electronic Engineering)

5 MARCH 2018
2:30 PM – 4:30 PM
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This question paper consists of 7 pages (4 pages with 4 questions and 3 pages for appendix).

2. Answer **ALL** questions. All necessary working steps must be shown.

3. Write all your answers in the answer booklet provided.

QUESTION 1 [25 Marks]

a) Define system bus and briefly describe three of its common functional group.

[4 marks]

b) Describe the process of memory **read** operation. Provide suitable illustration(s) to support your description.

[9 marks]

c) Based on the assembly language instructions below, answer the following questions:

```
            ORG 0050H
Line 1      MOV PSW, #18H
Line 2      MOV R1, #0A3H
Line 3      MOV R2, #57H
Line 4      MOV A, #91H
Line 5      MOV R3, #0F5H
Line 6      ADD A, R2
Line 7      MOV B, #10H
Line 8      MUL AB
            END
```

(i)   Which register bank is currently used?

[1 mark]

(ii)   After performing the instruction at **line 6**, what is the content of Carry Flag, Auxiliary Flag, Overflow Flag, Parity Flag, Accumulator and Program Status Word register?

[8 marks]

(iii)   What is the content of Accumulator and B after executing the instruction at **line 8**? Verify whether the OV flag is set or cleared and justify your reason.

[3 marks]

Continued...

QUESTION 2 [25 Marks]

Based on the given assembly language program at Table 1, answer the following questions:

Address	Line	Label	Instruction	Opcode	Addressing Mode	Instruction Type
			ORG 0000H			
0000	1		MOV R1,#0AH	(i)	(vi)	
0002	2	HERE:	MOV @R1,#00H	(ii)		
0004	3		INC R1	(iii)		
0005	4		NOP			
0006	5		MOV A, R1	(iv)	(vii)	
0007	6		CJNE R1,#35H,HERE		(viii)	(ix)
000A	7		SWAP A	(v)		(x)
			END			

Table 1

a) Complete the answer for the cells marked with roman numbers starting from (i) to (x).

[10 marks]

b) Find the opcode of the instruction at line 6. Please include your working step on finding the offset for the instruction at line 6.

[3 marks]

c) Calculate the total execution time of the program. The crystal frequency used is set to be 12 MHz.

[5 marks]

d) What is the content of the Accumulator and register R1 after executing the program?

[2 marks]

e) Reconstruct the assembly language program based on the given machine code at Table 2 below and state the final content of each of the affected memory locations. Include any proper labels if necessary.

Line	Opcode
1	78H 05H
2	79H 25H
3	09H
4	D8H FDH

Table 2

[5 marks]

Continued...

QUESTION 3 [25 Marks]

a) Construct an assembly language program to continuously monitor both motion sensor and infrared sensor connected to P2.5 and P2.6 respectively. A buzzer at P1.5 will turn ON for 0.5 seconds if the motion sensor is momentarily LOW, while an LED at P1.6 will turn ON for 0.5 seconds if the infrared sensor is momentarily LOW. If **both** sensors are LOW at the same time, always service and give priority to the motion sensor.

Use Timer 0 to provide delay for both buzzer and LED. Assume the crystal frequency used is 12 MHz. Note that the sensors, buzzer and LED are all set to be **active LOW. Do not use interrupt** and the working steps for calculation of timer reload value must be shown.

[15 marks]

b) Construct an assembly language program to continuously transmit the phrase "OVERFLOW" through serial port at 4800 bauds, whenever the infrared sensor connected to pin P2.6 is turned ON (Active LOW). Assume the crystal frequency used is 11.0592 MHz and the value of SMOD = 0. The working steps to calculate TH1 must be shown.

[10 marks]

Continued...

QUESTION 4 [25 Marks]

a) Briefly show the steps involved in interrupt processing.

[8 marks]

b) How to enable both serial port interrupt and external interrupt 1?

[1 mark]

c) Construct an assembly language program for the following requirements:

- A common anode 7-segment display is connected to P1 of an 8051 microcontroller. Turn ON the 7-segment display with character 'E', whenever the external interrupt $\overline{INT0}$ of pin P3.2 is LOW. Otherwise, turn OFF the 7-segment display.

- Right after the 7-segment display is turned OFF, the program must turn ON an LED 1 (Active LOW) connected to P1.5, for at least 20 milliseconds. The program should be able to repeat itself afterwards.

Apply edge-triggering to the external interrupt $\overline{INT0}$. Apply Timer 1 for the delay and assume 12MHz crystal frequency is used.

[16 marks]

End of Page.

APPENDIX A: OPCODE MAP

Instruction Code Summary

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	JBC bit,rel	JB bit,rel	JNB bit,rel	JC rel	JNC rel	JZ rel	JNZ rel	SJMP rel	MOV DPTR,#data16	ORL C,/bit	ANL C,/bit	PUSH dir	POP dir	MOVX A,@DPTR	MOVX @DPTR,A
1	AJMP (P0)	ACALL (P0)	AJMP (P1)	ACALL (P1)	AJMP (P2)	ACALL (P2)	AJMP (P3)	ACALL (P3)	AJMP (P4)	ACALL (P4)	AJMP (P5)	ACALL (P5)	AJMP (P6)	ACALL (P6)	AJMP (P7)	ACALL (P7)
2	LJMP addr16	LCALL addr16	RET	RETI	ORL dir,A	ANL dir,A	XRL dir,A	ORL C,bit	ANL C,bit	MOV bit,C	MOV C,bit	CPL bit	CLR bit	SETB bit	MOVX A,@R0	MOVX @R0,A
3	RR A	RRC A	RL A	RLC A	ORL dir,#data	ANL dir,#data	XRL dir,#data	JMP @A+DPTR	MOVC A,@A+PC	MOVC A,@A+DPTR	INC DPTR	CPL C	CLR C	SETB C	MOVX A,@R1	MOVX @R1,A
4	INC A	DEC A	ADD A,#data	ADDC A,#data	ORL A,#data	ANL A,#data	XRL A,#data	MOV A,#data	DIV AB	SUBB A,#data	MUL AB	CJNE A,#data,rel	SWAP A	DA A	CLR A	CPL A
5	INC dir	DEC dir	ADD A,dir	ADDC A,dir	ORL A,dir	ANL A,dir	XRL A,dir	MOV dir,#data	MOV dir,dir	SUBB A,dir		CJNE A,dir,rel	XCH A,dir	DJNZ dir,rel	MOV A,dir	MOV dir,A
6	INC @R0	DEC @R0	ADD A,@R0	ADDC A,@R0	ORL A,@R0	ANL A,@R0	XRL A,@R0	MOV @R0,#data	MOV dir,@R0	SUBB A,@R0	MOV @R0,dir	CJNE @R0,#data,rel	XCH A,@R0	XCHD A,@R0	MOV A,@R0	MOV @R0,A
7	INC @R1	DEC @R1	ADD A,@R1	ADDC A,@R1	ORL A,@R1	ANL A,@R1	XRL A,@R1	MOV @R1,#data	MOV dir,@R1	SUBB A,@R1	MOV @R1,dir	CJNE @R1,#data,rel	XCH A,@R1	XCHD A,@R1	MOV A,@R1	MOV @R1,A
8	INC R0	DEC R0	ADD A,R0	ADDC A,R0	ORL A,R0	ANL A,R0	XRL A,R0	MOV R0,#data	MOV dir,R0	SUBB A,R0	MOV R0,dir	CJNE R0,#data,rel	XCH A,R0	DJNZ R0,rel	MOV A,R0	MOV R0,A
9	INC R1	DEC R1	ADD A,R1	ADDC A,R1	ORL A,R1	ANL A,R1	XRL A,R1	MOV R1,#data	MOV dir,R1	SUBB A,R1	MOV R1,dir	CJNE R1,#data,rel	XCH A,R1	DJNZ R1,rel	MOV A,R1	MOV R1,A
A	INC R2	DEC R2	ADD A,R2	ADDC A,R2	ORL A,R2	ANL A,R2	XRL A,R2	MOV R2,#data	MOV dir,R2	SUBB A,R2	MOV R2,dir	CJNE R2,#data,rel	XCH A,R2	DJNZ R2,rel	MOV A,R2	MOV R2,A
B	INC R3	DEC R3	ADD A,R3	ADDC A,R3	ORL A,R3	ANL A,R3	XRL A,R3	MOV R3,#data	MOV dir,R3	SUBB A,R3	MOV R3,dir	CJNE R3,#data,rel	XCH A,R3	DJNZ R3,rel	MOV A,R3	MOV R3,A
C	INC R4	DEC R4	ADD A,R4	ADDC A,R4	ORL A,R4	ANL A,R4	XRL A,R4	MOV R4,#data	MOV dir,R4	SUBB A,R4	MOV R4,dir	CJNE R4,#data,rel	XCH A,R4	DJNZ R4,rel	MOV A,R4	MOV R4,A
D	INC R5	DEC R5	ADD A,R5	ADDC A,R5	ORL A,R5	ANL A,R5	XRL A,R5	MOV R5,#data	MOV dir,R5	SUBB A,R5	MOV R5,dir	CJNE R5,#data,rel	XCH A,R5	DJNZ R5,rel	MOV A,R5	MOV R5,A
E	INC R6	DEC R6	ADD A,R6	ADDC A,R6	ORL A,R6	ANL A,R6	XRL A,R6	MOV R6,#data	MOV dir,R6	SUBB A,R6	MOV R6,dir	CJNE R6,#data,rel	XCH A,R6	DJNZ R6,rel	MOV A,R6	MOV R6,A
F	INC R7	DEC R7	ADD A,R7	ADDC A,R7	ORL A,R7	ANL A,R7	XRL A,R7	MOV R7,#data	MOV dir,R7	SUBB A,R7	MOV R7,dir	CJNE R7,#data,rel	XCH A,R7	DJNZ R7,rel	MOV A,R7	MOV R7,A

Legend:
- 2Byte / 2Cycle
- 3Byte / 4Cycle

APPENDIX B: 8051 SPECIAL FUNCTION REGISTER (SFR)

Byte address	Bit address								
FF									
F0	F7	F6	F5	F4	F3	F2	F1	F0	B
E0	E7	E6	E5	E4	E3	E2	E1	E0	ACC
D0	D7	D6	D5	D4	D3	D2	D1	D0	PSW
B8	--	--	--	BC	BB	BA	B9	B8	IP
B0	B7	B6	B5	B4	B3	B2	B1	B0	P3
A8	AF	--	--	AC	AB	AA	A9	A8	IE
A0	A7	A6	A5	A4	A3	A2	A1	A0	P2
99	not bit addressable								SBUF
98	9F	9E	9D	9C	9B	9A	99	98	SCON
90	97	96	95	94	93	92	91	90	P1
8D	not bit addressable								TH1
8C	not bit addressable								TH0
8B	not bit addressable								TL1
8A	not bit addressable								TL0
89	not bit addressable								TMOD
88	8F	8E	8D	8C	8B	8A	89	88	TCON
87	not bit addressable								PCON
83	not bit addressable								DPH
82	not bit addressable								DPL
81	not bit addressable								SP
80	87	86	85	84	83	82	81	80	P0

Special Function Registers

SFR RAM Address (Byte and Bit)

APPENDIX C: BIT-ADDRESSABLE RAM LOCATIONS

Byte Address	Bit Address							
2F	7F	7E	7D	7C	7B	7A	79	78
2E	77	76	75	74	73	72	71	70
2D	6F	6E	6D	6C	6B	6A	69	68
2C	67	66	65	64	63	62	61	60
2B	5F	5E	5D	5C	5B	5A	59	58
2A	57	56	55	54	53	52	51	50
29	4F	4E	4D	4C	4B	4A	49	48
28	47	46	45	44	43	42	41	40
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	09	08
20	07	06	05	04	03	02	01	00

APPENDIX D: PROGRAM STATUS WORD (PSW)

CY	AC	F0	RS1	RS0	OV	--	P

APPENDIX E: TIMER/COUNTER MODE CONTROL (TMOD) REGISTER

G	C/T	M1	M0	G	C/T	M1	M0

APPENDIX F: SERIAL CONTROL (SCON) REGISTER

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

APPENDIX G: INTERRUPT ENABLE (IE) REGISTER

EA	--	ET2	ES	ET1	EX1	ET0	EX0

APPENDIX H: INTERRUPT PRIORITY (IP) REGISTER

--	--	PT2	PS	PT1	PX1	PT0	PX0